

56-Gb/s Silicon Optical Receiver using a Low-Noise Fully-Differential Transimpedance Amplifier in SiGe BiCMOS

Joris Lambrecht⁽¹⁾, Hannes Ramon⁽¹⁾, Bart Moeneclaey⁽¹⁾, Jochem Verbist^(1,2), Peter Ossieur⁽¹⁾, Peter De Heyn⁽³⁾, Joris Van Campenhout⁽³⁾, Johan Bauwelinck⁽¹⁾, Xin Yin⁽¹⁾

⁽¹⁾ Ghent University - imec, IDLab, INTEC, 9052 Ghent, Belgium, joris.lambrecht@ugent.be

⁽²⁾ Ghent University - imec, Photonics Research Group, INTEC, 9052 Ghent, Belgium

⁽³⁾ imec, 3001 Leuven, Belgium

Abstract We present a silicon optical receiver consisting of a low-noise fully-differential transimpedance amplifier with on-chip biasing for a SiPh Ge PD. Error-free ($BER < 10^{-12}$) 56Gb/s NRZ operation is demonstrated with a record OMA sensitivity of -10.2dBm at 170mW.

Introduction

Industry is now targeting 800G and 1.6T links for data centers, while also considering on-board optics to replace electrical links^{1,2}. Transceivers for such applications need to be integrated into small form factors containing a high number of parallel channels, have good energy efficiency and per-channel bitrates of at least 50Gb/s. For the receiver (RX) good sensitivity is required, which improves the link budget. This can be used to lower the laser output power, thus reducing power consumption and improving lifetime. While >50Gb/s RXs, tested in real-time optical bit-error rate (BER) measurements, have been demonstrated³⁻⁶; these have either a high power consumption or moderate sensitivity.

We present an optical RX built around a 55 nm SiGe BiCMOS transimpedance amplifier (TIA) featuring a novel fully-differential photodiode (PD) current sensing and on-chip PD biasing. The TIA was wirebonded to a silicon photonic (SiPh) 0.8A/W, low-capacitance (30fF) integrated waveguide Ge photodiode (PD)⁷. Thanks to the differential operation and the very low PD capacitance, the TIA achieves high gain (72.5dB Ω) and low-noise, resulting in -10.2dBm optical modulation amplitude (OMA) sensitivity ($BER < 10^{-12}$) and -14.1dBm at KP4-FEC ($BER < 2.4 \times 10^{-4}$) at 56Gb/s. To the best of our knowledge, this is the best sensitivity at a low power consumption demonstrated for such

optical RXs.

Receiver architecture

The high-speed input of the TIA is typically connected to either the anode or cathode of the PD, while the other PD pin is connected to a bias voltage. The RX sensitivity can be improved by processing the PD current (I_{PD}) differentially, using both cathode and anode as high-speed inputs. Sensing I_{PD} differentially doubles the TIA gain and improves the signal-to-noise-ratio by $\sqrt{2}$. The increased front-end gain reduces the contribution of the amplifying stages to the total input referred noise and also reduces their gain requirement by 6dB. This lowers the power consumption as less gain stages are required. Differential PD sensing also doubles the effective PD capacitance but for high-speed PDs this capacitance is very low. Furthermore, differential PD sensing requires a low-noise biasing network that provides a low-impedance path for the DC photocurrent. This can be done using an RC bias-T⁸. However large (e.g. 1-2k Ω) resistors are required to minimize the noise current penalty and keep the loop gain of the input stage high enough. Consequently, a significant voltage drop (several Volts) develops over these resistors as $I_{PD,DC}$ increases. To avoid bandwidth degradation, sufficient reverse bias (e.g. 2V) needs to be maintained over the PD at all $I_{PD,DC}$ (e.g. up to 1mA) and all I_{PD} signal swings, thus requiring a larger bias voltage (e.g. > 4V), which may not be available in small

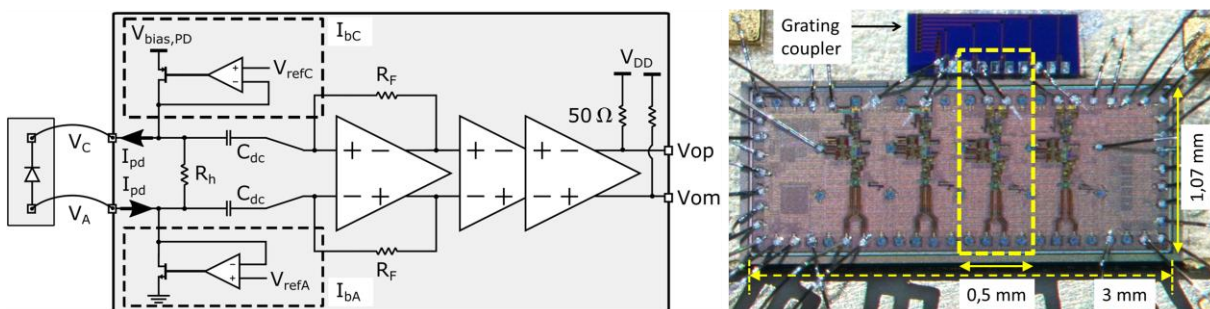


Fig. 1: (a) Differential receiver block diagram (b) TIA and PD wirebonded to a test PCB, the tested channel is highlighted.

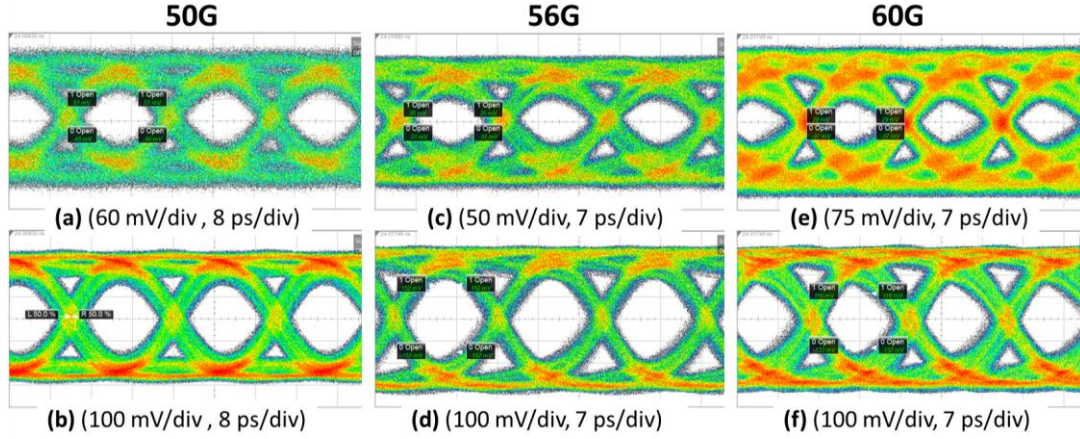


Fig. 2: 50 Gb/s differential TIA eye at (a) -12 dBm OMA and (b) -7 dBm OMA at 100 μA I_{ref} . 56 Gb/s differential TIA eye at (c) -12 dBm and (d) -6 dBm OMA at 110 μA I_{ref} . 60 Gb/s TIA eye at (e) -10 dBm and (f) -6 dBm OMA at 110 μA I_{ref} .

modules. Fig. 1.a shows a block diagram of the proposed TIA that solves this problem. The employed on-chip biasing network consists of opamp-controlled current sources I_{bC} and I_{bA} and on-chip DC-blocks C_{dc} . The photodiode bias $V_C - V_A$ is digitally programmed by means of reference voltages V_{refC} and V_{refA} , implemented as on-chip voltage DACs. The input stage biasing is not affected by the PD bias due to DC-blocks C_{dc} . Conversely, for the signal frequencies of interest, I_{bC} and I_{bA} present high impedances and the signal current flows through the DC-blocks into the input stage. This network offers several advantages over the RC bias-T.

Firstly, as long as the voltage across I_{bC} and I_{bA} is higher than $\sim 0.4\text{V}$, the opamp feedback loops keep V_C and V_A at V_{refC} and V_{refA} respectively. Compared to the RC bias-T, $V_{\text{bias,PD}}$ can therefore be reduced significantly. Secondly, since V_{refC} and V_{refA} are generated from clean reference voltage DACs, low-frequency interferences on the ground or $V_{\text{bias,PD}}$ (common issue in multi-channel receivers) should not affect the bias voltage over the PD. High-frequency interference can be eliminated by sufficient on-chip supply decoupling between $V_{\text{bias,PD}}$ and ground. Thirdly, the feedback introduced by the opamps reduces the low-frequency input impedance of the TIA, ensuring a stable and sufficient reverse bias for a large range of I_{pd} (designed up to 2mA DC photocurrent here). Fourthly, at very small input signals, I_{bC} and I_{bA} need to provide only a very small current. Therefore, their contribution to the input referred noise is very small when it is most critical, at the weakest input signals.

The input stage is followed by an amplifier and a 50 Ω output stage. The bias currents of all stages are controlled with an external bias current I_{ref} , which is used to tune the TIA performance and power consumption. Nominally, I_{ref} is set to 100 μA and the TIA draws 58mA from a 2.5V supply.

Experimental setup

The TIA chip was fabricated in a 55 nm SiGe BiCMOS technology. The TIA is wirebonded to a SiPh integrated circuit containing a grating coupler and a Ge PD from imec's iSIPP50G platform⁷ (Fig. 1.b). The PD supply voltage is set to 2.8V, resulting in $\sim 2\text{V}$ effective reverse bias over the PD. 50Gb/s and 56Gb/s 2^9-1 pseudo-random binary (PRBS) input signals are generated by a M8196A 92 GSa/s Arbitrary Waveform Generator (AWG). A 1550nm laser is modulated by a Mach-Zehnder modulator (FTM7937EZ), driven by a 50GHz RF amplifier. The optical transmit eyes, detected with a 70GHz DC-coupled PD, are shown in Fig. 3. The measured extinction ratio was $>10\text{dB}$ for all data rates. The modulated light is coupled into a C-band grating coupler (loss $\sim 6\text{ dB}$) via a fiber probe. The output of the TIA is measured with a 67GHz GSSG-probe. The BER is measured by a 50Gb/s SHF 11100B error analyser (EA). Still, error-free operation was measured at 56Gb/s. Every BER is acquired after at least 10 bit errors have occurred. Eye diagrams and TIA noise measurements are obtained using a Keysight DCA 86100D sampling scope with remote sampling heads (set to 50GHz bandwidth).

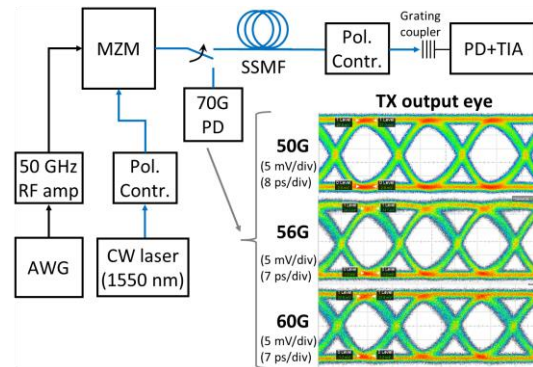


Fig. 3: Experimental setup.

Tab. 1: Comparison with prior published optical receivers tested with real-time BERT.

	Bit rate [Gb/s]	P _{dc} [mW]	R _F [dBΩ]	R [A/W]	OMA KP4 [dBm]	OMA 10 ⁻¹² [dBm]	PRBS	pJ/b	Technology & remarks	
[3]*	56	165	N/A	1	-8.5*	N/A (> -1)	2 ⁹ -1	2.94	130 nm BiCMOS	
[4]*	50	395	70	0.8	-13*	-9.2	2 ⁹ -1	7.9	180 nm BiCMOS	
[5]	50	860	N/A	0.48	-12.2	-9.8	2 ⁷ -1	17.2	130 nm BiCMOS	
	64		N/A		-9*	-7		13.4		
[6]	40	158	70	0.55	-11.5	-6.4	2 ³¹ -1	3.95	130 nm BiCMOS	
This work	50	130	72	0.8	-14.2	-8.4	2 ⁹ -1	2.6	55 nm BiCMOS, I _{ref} = 90μA	
	50	170	72.5		-15.2	-10.6		3.4		I _{ref} = 120μA
	56**	170	72.5		-14.1	-10.2		3		I _{ref} = 120μA
*BER Extrapolated to KP4-FEC **BERT only rated up to 50Gb/s										

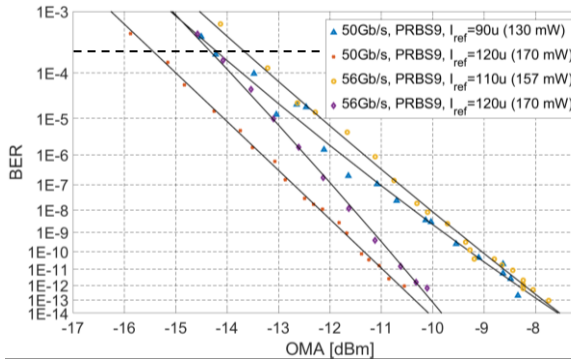


Fig. 4: BER at 50Gb/s and 56Gb/s.

Results and discussion

The TIA transimpedance is calculated as the ratio of the measured output swing to the input current swing, resulting in 72.5dBΩ (4.2kΩ) at 56Gb/s. The differential TIA output eyes are shown in Fig. 2. Input-referred noise current is determined by measuring the TIA output noise when no optical signal is applied; subtracting the contribution of the scope and dividing by the measured TIA gain. This gives ~2.2μA_{RMS} at 100μA I_{ref}.

In Fig. 4, The BERs are plotted vs. the OMA. The latter is referred to the input of the photodiode using the measured average photocurrent, the measured ER and the PD responsivity. By setting I_{REF} to 120μA, error-free (BER<10⁻¹²) operation is shown at 56Gb/s (50Gb/s) with a sensitivity of -10.2dBm (-10.6dBm) OMA, while consuming 170mW. Sub-KP4-FEC 56Gb/s (50Gb/s) operation is obtained at -14.1dBm (-15.2 dBm) OMA. Reducing I_{ref} to 110μA results in a lower power consumption of 157mW but also lowers the sensitivity for a BER of 10⁻¹² to -8.2dBm OMA. Further reducing I_{ref} to 90 μA yields a low-power mode (130 mW), achieving error-free 50Gb/s-operation at -8.4dBm OMA and sub-KP4-FEC performance at -14.2dBm OMA. Although open eyes are shown at 60Gb/s in Fig.2, no BERs could be measured due to limitations of our 50Gb/s EA.

In Tab.1, we compare our BER results with current state-of-the-art receivers. For 120μA I_{REF}, our receiver achieves the best sensitivity for both BER-limits at the second-lowest power consumption. With I_{REF} set to 90μA, we obtain the best energy efficiency at 50Gb/s, with good sensitivity.

Conclusion

We have presented a silicon optical receiver consisting of a 50GHz, 0.8 A/W SiPh PD wirebonded to a fully-differential TIA in 55 nm BiCMOS. Compared to state-of-the art receivers tested with optical real-time BERT, our receiver achieves a record OMA sensitivity of -10.2dBm at 56Gb/s, while consuming only 170mW.

Acknowledgements

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